Research of innovative solutions for the implementation of pinned photodiodes in high resistive substrates for near infrared and particle detection

Department: Electronics, Optronics and Signal (DEOS)

This project consists in analysing and understanding the performance of CMOS imagers based on pinned photodiodes and made on high resistive silicon substrates. These substrates, more resistive than "usual" ones, offer a deeper carrier collection and are very attractive for near infrared imaging applications. However, the evolution of the pixel performances is unknown on a such material; in particular a degradation in charge transfer quality and a change in the pinning voltage are expected.

The challenge is to have a CMOS imager with increased sensitivity in the red and near infrared for a wider spectral band, while keeping the high performances of modern CMOS image sensors based on pinned photodiodes. The aim of this PhD is therefore to investigate how are modified the key parameters, propose new models and develop strategies in order to maintain pixel high performances.

JOB DESCRIPTION:

CMOS image sensors currently developed for consumer devices (smartphone, camera), but also for advanced scientific applications such as Earth observation, use pixel arrays with so-called "pinned" photodiodes. "Pinned" photodiodes (PPD) are devices that appeared almost 30 years ago and are widely used nowadays thanks to their very good performances in dark current and sensitivity. Indeed, these photodiodes, due to their construction, have the collection region (N cathode) isolated from the interface and its surface oxide by a pinning layer (P-doped) (see Fig. 1), which drastically limits the formation of dark current during the integration of the photonic signal.

These devices are made on silicon wafers like the vast majority of microelectronic components. The silicon has the advantage of having a band gap energy of 1.12 eV, which leads to the existence of a cut-off frequency of silicon equal to about 1.1 µm. As the very short wavelengths are also absorbed in the surface layers before reaching the silicon, it follows that CMOS on silicon devices can detect photons between 400 nm and about 900 nm.

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The best performances in photon detection sensitivity (also called quantum efficiency, QE) are thus obtained between 450 nm and 650 nm, which corresponds to a generation depth of electron-hole pairs in the first µm. On the other hand, the photodiode dopant layers rarely exceed 1.5 µm, and the depletion region created by the reverse biasing of the photodiode extend over ~2 µm in depth with usual substrates. The depletion region depth is essential for the image sensor sensitivity as it defines the region having an electric filed able to efficiency collect photodegenerated charges. Thus, the photon detection sensitivity quickly drops for wavelengths above 650 nm. It is then very difficult to efficiently detect photons in the near infrared.

However, there are needs requiring to make images in the near infrared or also to increase the sensitivity in all the wavelength range, in particular for military applications. The targeted applications are, for example, the detection of bodies emitting in the near infrared, but also devices using polarization imagers for which the sensitivity becomes very weak as soon as a polarization direction is selected, or the development of pixels for particle detections (for electron microscope or Xray experiment for instance). Therefore, these detectors need an increased sensitivity to the light and especially into the near infrared wavelengths.

One way to increase the sensitivity of CMOS imagers and in particular in the near infrared is to increase the depth of the depleted region created by the photodiode. The only possible solution is then to use resistive substrates rather than increasing the bias voltage of the photodiode (Thesis of Jean Baptiste Lincelles, ISAE, 2016). Until now, no study has been performed on the influence of substrate resistivity on PPD parameters, except the analysis of its better collection on the near infrared due to the increased depletion depth. While the PPD offers very attractive performances, it is thus necessary to study the evolution of its key parameters (pinning voltage, full well capacity, QE, dark current, lag, readout noise, radiation tolerance) when the substrate is resistive, even very resistive.

The challenge of this thesis is therefore to study pinned photodiodes on different resistive substrates using TCAD simulations and analytical models to demonstrate a good understanding of the phenomena, but also to perform some measurements on CMOS pixel arrays. The candidate will thus study all the parameters of the pixel on atypical substrates and will investigate by means of physical models and measurements the root cause of eventual degradations in order to propose new design rules and new models for key parameters. The final goal will be to be able to realize future CMOS image sensors for near infrared vision or particle detection.

PROGRAM:

CMOS processes developed for imaging applications have the major advantage of photodetectors optimized in terms of dark current and noise [3] (devices known as pinned photodiode offering screening with respect to interface traps) and transmission of silicon photons through an optimized dielectric layer thanks to anti-reflective layers.

The proposed thesis work mainly aims to understand how the key parameters of the pinned photodiode pixel evolve as a function of the resistivity of the substrate, and to propose some rules for improving the pixel design is such case. These parameters are the pinning voltage [1], i.e. the potential of the depleted photodiode relatively to the substrate, the lag or the charge transfer inefficiency between the photodiode and the sense node [2] , the full well capacity of the photodiode [1], the dark current, the readout noise, and above all the quantum efficiency (QE) which measures the sensitivity of the pixel as a function of the wavelength. Measurements will be conducted on CMOS image sensors developed at ISAE-SUPAERO on various substrates. These measurements will be compared with models and TCAD simulations with the aim to understand all the physical phenomena at the root cause of parameter modifications. Until now, some analytical models have been developed concerning the full well capacity, the pinning voltage. The candidate will have to modify these models in order to consider the substrate doping, and eventually propose new models for the other parameters.

Then, the PhD student will have to determine how the design of pixels must be modified, by shifting or modifying layers, in order to realize high performance pinned photodiodes on a very resistive substrate. In the case of particle detection, it is also interesting to estimate the evolution of radiation tolerance of pinned photodiodes according to various substrates, knowing that electron lifetime influencing the dark current depends on the substrate doping. It is thus expected that the radiation tolerance might be modified with high resistive substrates. Currently there are works related to pinned photodiodes in resistive substrate [4-6], but there is no analysis of the characteristics of the photodiode, nor a quantitative comparison between different substrate doping concentrations.

Finally, no study presents the possible modifications that will have to be considered to produce such imagers, which could be applied to any imaging technology. The student will rely on the work of J. B. Lincelles who did a thesis at ISAESUPAERO on "3T" type imagers (without pinned photodiode) in very resistive substrate [7], and which constitutes a solid base to start this thesis. To carry out this study, the candidate will have at his disposal TCAD simulation tools (see example in Fig. 2), widely used in the microelectronic industry to anticipate and understand the behavior of devices and also to understand the physics controlling the movement and collection of charges.

On the other hand, the candidate will have the possibility to measure pixels arrays based on pinned photodiodes and made on different substrates whose resistivity will range from "normal" (1015B/cm3) values to very resistive values (1013B/cm3). These imagers are already available, and will be measured and analysed on ISAE-SUPAERO's electro-optical benches in a clean room environment.

For exploring the radiation tolerance of such image sensors, the PhD student will have the possibility to use our proper irradiation facility based on an X ray chamber.

Suggested planning :

• Conduct a bibliography review of the state of the art concerning:
  - o CMOS technologies optimized for imaging applications
  - o Key parameters of pinned photodiode pixels
  - o Review of the work done on resistive substrate imagers

• Understand by using simple analytical models or TCAD simulations the eventual influence of the substrate resistivity on parameters of the imager

• Carry out measurement campaigns on the pixel arrays available at ISAE to correlate simulated results with experimental observations, analyse the eventual improvements in imager performance as a function of substrate doping.

• Propose new models for key parameters, analyse the eventual issues induced by the use of resistive substrates and propose innovative solutions to circumvent them.

• Propose new design rules for resistive substrate imagers as well as ways of improvement.

• Study the radiation tolerance of pinned photodiode image sensors based on more resistive substrates.

REQUIRED PROFILE:
Master Degree addressing one or several of the following themes :
• Solid State Physics / Semiconductor Physics / Semiconductor Device Physics
• Nano-Microelectronics / Optoelectronics
• Semiconductor physic

FUNDING : DGA-AID Classique / ISAE-SUPAERO

LOCATION: ISAE-SUPAERO, Toulouse

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REFERENCES:

[1] A. Pelamatti ; Comparison of Pinning Voltage Estimation Methods in Pinned Photodiode CMOS Image Sensors, 2015

[2] X. Chao, Design and Optimization of Four-Transistor Pixel for Low Image Lag CMOS Image Sensor, 2013

[3] E. Fossum, A Review of the Pinned Photodiode for CCD and CMOS Image Sensors, 2014

[4] K. Stefanov, Design and Performance of a Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias, Sensors, 2018

[5] X. Meng, Radiation Hardness Study on a Fully Depleted Pinned Photodiode CMOS Image Sensor, 2019

[6] X. Fang, Analyses of Pinned Photodiodes With High Resistivity Epitaxial Layer for Indirect Time-of-Flight Applications, 2020

[7] J .B Lincelles, Enhanced Near-Infrared Response CMOS Image Sensors Using HighResistivity Substrate: Photodiodes Design Impact on Performances, 2016