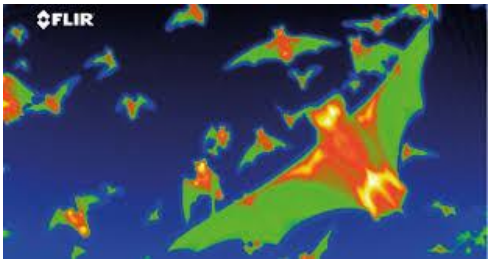
Research of innovative solutions for the implementation of pinned photodiodes in high resistive substrates for infrared detection.



Funding: DGA-AID Classique

Location: ISAE-SUPAERO, Toulouse

1. PhD goal

This study consists in analysing and understanding the performance of imagers based on pinned photodiodes made on silicon substrates that are more resistive than “normal” ones. The challenge is to have a CMOS imager with increased sensitivity in the red and near infrared to increase the spectral band while keeping the advantages of CMOS devices on silicon.

2. PhD subject description

CMOS image sensors currently used on consumer devices (smartphone, camera), but also for advanced scientific applications such as Earth observation, use pixel arrays with so-called “pinned” photodiodes. “Pinned” photodiodes (PPD) are devices that appeared almost 30 years ago and are widely used nowadays thanks to their very good performance in dark current and sensitivity. Indeed, these photodiodes, due to their construction, have the collection region (N cathode) isolated from the interface and its surface oxide by a pinning layer (P-doped) (see Fig. 1), which limits drastically the formation of dark current during the integration of the photonic signal.

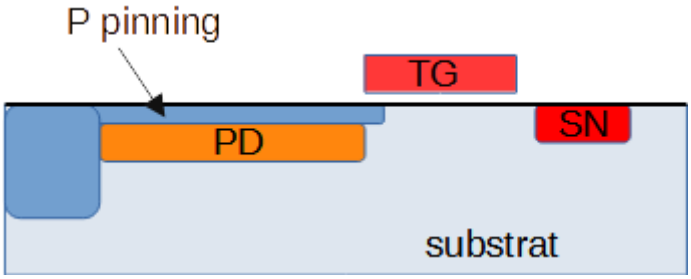


Fig. 1 Schematic cross-section of a pinned photodiode. TG is the transfer gate, SN the collection node and PD the photodiode.

These devices are made on silicon wafers like the vast majority of microelectronic components. Silicon has the advantage of having a band gap energy of 1.12 eV, which leads to the existence of a cut-off frequency of Silicon equal to about 1.1 µm. As the very short wavelengths are also absorbed in the surface layers before reaching the silicon, it follows that CMOS on silicon devices can detect photons between 400 nm and about 900 nm.

The best performances in photon detection sensitivity (also called quantum efficiency, QE) are thus obtained between 450 nm and 650 nm, which corresponds to a generation depth of electron-hole pairs that is reasonable and compatible with the depths of the components realized. in the substrate. Indeed, the dopant layers rarely exceed 1.5 μm, and the depletion zones created by the reverse biasing of the photodiode extend over 2 μm in depth with usual substrates. These depletion regions are essential for the charge collection generated by the photons, because it is in these regions that there is an electric field capable of efficiently collecting the photo-generated charges. Thus, the photon detection sensitivity decreases quickly for wavelengths above 650 nm. It is then very difficult to effectively detect photons in the near infrared with pixels made on silicon substrates.

However, there are needs requiring to make images in the near infrared or in a simpler way to make it possible to increase the sensitivity in all the wavelength range, in particular for military applications. The targeted applications are, for example, the detection of bodies emitting in the near infrared, but also devices using polarization imagers for which the sensitivity becomes very low as soon as a polarization direction is selected, or the development of pixels with very high gain which need to maximize charge collection to achieve single photon detection. These detectors have therefore an increased sensitivity to light and a spectral band which can be extended into the near infrared. This way of improving detection in the near infrared will make it possible to detect wavelengths up to 950 nm and therefore to avoid using materials other than silicon.

One way to increase the sensitivity of CMOS imagers and in particular in the near infrared is to increase the depth of the depleted region created by the photodiode. The only possible solution is then to use resistive substrates rather than increasing the bias voltage of the photodiode (Thesis of Jean Baptiste Lincelles, ISAE, 2016). However, there is no comprehensive study in the literature analyzing the behavior of the key parameters (pinning voltage, full well capacity, QE, dark current, lag) of the pinned photodiode when it is made on resistive substrates, even very resistive. **The challenge of this thesis is therefore to study pinned photodiodes on different resistive substrates using TCAD simulations, analytical models to demonstrate a good understanding of the phenomena, but also measurements on pixel arrays. The candidate will thus study all the parameters of the pixel on atypical substrates and will analyze the compromises and the future design rules necessary for the realization of integrated devices.**

3. PhD program

The proposed thesis work mainly aims to understand how the key parameters of the pinned photodiode pixel evolve as a function of the resistivity of the substrate. These parameters are the pinning voltage [1], i.e. the potential of the depleted photodiode relatively to the substrate, the lag or the charge transfer inefficiency between the photodiode and the sense node [2] , the full well capacity of the photodiode [1], the dark current, the readout noise, and above all the quantum efficiency (QE) which measures the sensitivity of the pixel as a function of the wavelength. The study will be carried out by taking advantage of the capabilities of the CMOS processes developed by the founders for imaging applications. These have the major advantage of photodetectors optimized in terms of dark current and noise [3] (devices known as pinned photodiode offering screening with respect to interface traps) and transmission of silicon photons through an optimized dielectric layer thanks to anti-reflective layers.

The challenge is to be able to analyze and explain how the doping of the substrate influences the key parameters of the imager and to define what are the limits to the use of resistive substrates for pinned photodiodes. Then, the PhD student will have to determine how the design of the pixel must be modified (from the point of view of the usage of available dopant layers or if certain layers must be modified) to allow its use on a very resistive substrate.
Currently there are some works on pinned photodiodes in resistive substrate [4-5], but there is no analysis of the characteristics of the photodiode, nor a comparison between different substrate doping concentrations. Finally, no study presents the possible modifications that will have to be taken into account to produce such imagers. The student will rely on the work of J. B. Lincelles who did a thesis at ISAE-SUPAERO on "3T" type imagers (without pinned photodiode) in very resistive substrate [6], and which constitutes a solid base to start this thesis.

To carry out this study, the candidate will have at his disposal TCAD simulation tools (see example in Fig. 2), widely used in the microelectronic industry to anticipate the behavior of components and also to understand the physics governing the phenomena of movement and collection of charges.

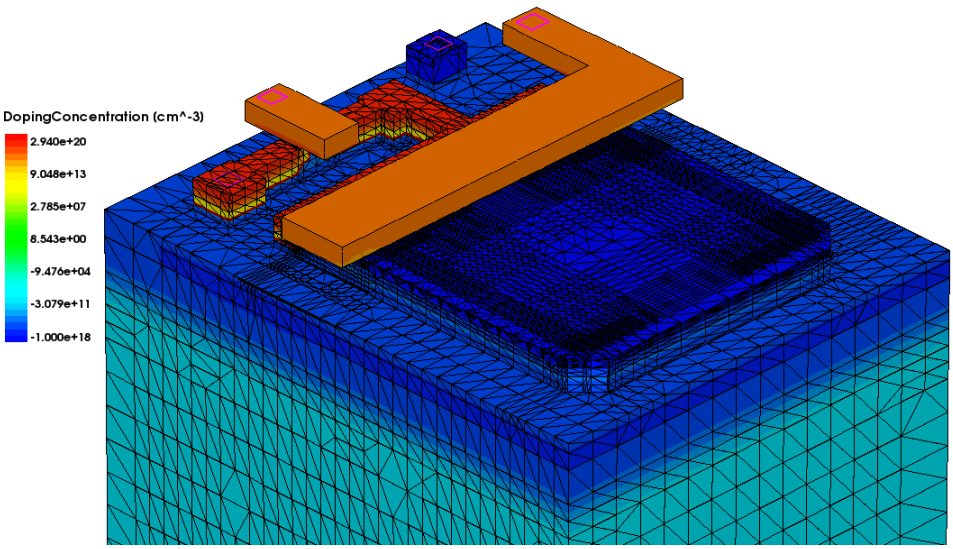


Fig. 2 3D TCAD simulation of a pinned photodiode pixel.

On the other hand, the candidate will have the possibility to measure pixels arrays based on pinned photodiodes and made on different substrates whose resistivity will range from "normal" values to very resistive values. These imagers can be measured and analyzed on ISAE-SUPAERO's electro-optical benches, and will make it possible to carry out the first analyzes which will eventually lead to the production of another test vehicle.

Planning :

- Conduct a bibliography review of the state of the art concerning:
  - CMOS technologies optimized for imaging applications
  - Key parameters of pinned photodiode pixels
  - Review of work done on resistive substrate imagers

- Understand by using simple analytical models or TCAD simulation what kind of influence the resistivity of the substrate can have on parameters of the imager
- Carry out measurement campaigns on the pixel arrays available at ISAE to correlate simulated results with experimental observations, analyze the eventual improvements in imager performance as a function of substrate doping.
- Propose new models for key parameters, analyze the issues induced by the use of resistive substrates and propose innovative solutions to circumvent them.
- Propose new design rules for resistive substrate imagers as well as ways of improvement. An imager may eventually be designed based on the conclusions drawn.

[1] A. Pelamatti ; Comparison of Pinning Voltage Estimation Methods in Pinned Photodiode CMOS Image Sensors, 2015
[2] X. Chao, Design and Optimization of Four-Transistor Pixel for Low Image Lag CMOS Image Sensor, 2013
[3] E. Fossum, A Review of the Pinned Photodiode for CCD and CMOS Image Sensors, 2014
[4] K. Stefanov, Design and Performance of a Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias, Sensors, 2018
[5] X. Meng, Radiation Hardness Study on a Fully Depleted Pinned Photodiode CMOS Image Sensor, 2019
[6] J .B Lincelles, Enhanced Near-Infrared Response CMOS Image Sensors Using High-Resistivity Substrate: Photodiodes Design Impact on Performances, 2016

4. Required competences

Master Degree addressing one or several of the following themes :
- Solid State Physics / Semiconductor Physics / Semiconductor Device Physics
- Nano-Microelectronics / Optoelectronics
- Semiconductor physic

5. How to apply?

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