PhD position @ ISAE-SUPAERO

Analysis and design of CMOS Image Sensors operated at cryogenic temperatures

Thesis advisors: Pierre Magnan (ISAE/DEOS/CIMI), Philippe Martin-Gonthier (ISAE/DEOS/CIMI)

Contact: pierre.magnan@isae-supaero.fr philippe.martin-gonthier@isae-supaero.fr

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Summary: For space science applications, such as astronomy [1]-[3], despite the extremely low read noise achieved by CMOS image sensors and the improvement of their dark current, there remains a need to further reduce the dark current noise by operating the sensors at low temperature or even cryogenic (as it is the case for the best CCD sensors). This would bring the noise coming from the dark current to a negligible level compared to the read noise for long exposures. A dark current value as low as 2.10^{-3} e/s was thus obtained at 200K from a CMOS image sensor manufactured with a 0.18µm CIS technology with a 7µm pixel pitch.

However, the behavior at very low temperatures and cryogenic temperatures of modern CMOS image sensors using Pinned Photodiodes has so far not been studied in depth and in all its aspects. The operation of CMOS devices at cryogenic temperature modifies several mechanisms and parameters of the semiconductor: reduction of the Bandgap (which slightly modifies the cut-off wavelength), increase of mobility of the carriers and their drift velocity, but also the incomplete ionization of the doping impurities. This impacts both the Pinned Photodiode and the associated Transfer Gate but also the MOS devices of the pixel, leading to several changes in pixel characteristics.

Preliminary investigations [4] have shown that due to changes in electrostatic conditions within the low temperature pixel, the diode potential (pinning voltage) is significantly reduced at low temperature (50% to 80K). This potentially affects the Full Well Charge unless the capacity of the Pinned Phodiode increases, which has not been analyzed to date. It has also been shown that the usual TCAD simulation (Deck) environment is not representative of the operation of low temperature devices. An improved TCAD model is required to take into account the incomplete ionization of dopants in order to obtain a good correlation between simulations and measurements. A suitable methodology, test structures and ad-hoc characterization methods to extract the characteristic parameters, is to be developed in order to have a valid tool for analyzing the electrostatic conditions in the region of the PPD and its Transfer Gate. This is of primary importance to confirm what preliminary investigations have shown: the absence of potential pockets and potential barriers that could prevent full charge transfer from the PPD to the readout node, thereby generating remanence at low temperature. However, this point has not been confirmed experimentally due to lack of work, and the transfer efficiency at low temperature is still an open question. Moreover, thanks to the increase in carrier mobility in the Transfer Gate channel, an increase in the transfer speed can be expected, but this has not been up to now demonstrated neither or unvalidated.

Since the characteristics of the MOS transistors (whether in the pixel or in the readout circuit) are significantly modified at low temperature because of the two antagonistic mechanisms - the increase of the threshold voltage and the increase of carrier mobility in the channel, the transfer function of the reading chain must be carefully analyzed with caution in multiple bias configurations. As it is well known that the BSIM models of CMOS foundries are not valid below -55°C, an adequate methodology based on test structures, the selection of the adapted model (EKV, PSP…) and the extraction parameters associated with cryogenic temperature must be developed to analyze the readout chain by electrical simulation. Finally, the improvement of the understanding of the operation of the low-temperature PPD thanks to the in-depth analysis of the previous points, will lead to the development of guidelines for the design of CMOS imager pixels optimized for operation at low temperature and cryogenic temperature.

[1] A. Hammoud and al. "Electronic components and circuits for extreme temperature environments" ICECS 2003, pp 44 - 47

[2] S-Y. Wang and al, " The prototype cameras for trans-Neptunian automatic occultation survey ", *Proc. SPIE* 9908, Ground-based and Airborne Instrumentation for Astronomy VI, 990846 (August 2016)

[3] J. Pratlong and al, "A 9 megapixel large-area back-thinned CMOS sensor with high sensitivity and high frame-rate for the TAOS II program ", *Proc. SPIE* 9915, High Energy, Optical, and Infrared Detectors for Astronomy VII, 991514 (August 2016)

[4] Ph. Martin-Gonthier, P. Magnan, O. Marcelot, “Investigations on cryogenic operation of Pinned photodiode pixels”, International Image Sensor Workshop 2017, Hiroshima, June 2017