Research topic proposal for PhD Position at ISAE-SUPAERO, AIRBUS DS & ESA

Exploration of Hot Carrier Injection mechanisms and impact mitigation by design techniques for InfraRed Focal Plane Array operated at cryogenic temperatures

PhD position proposed by ISAE-SUPAERO, Airbus Defense & Space and ESA

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Main location : ISAE-SUPAERO, Toulouse, France

Scientific field: Semiconductor Physics, Micro and Nanotechnology

Keywords: Cryogenic temperature, Infrared detectors, Microelectronic design, Hot carrier injection, aging, electroluminescence, photon emission, blooming, glow effect, Random Telegraph Noise

Context:

Infrared (IR) imaging systems are widely used in civilian and military settings like spectroscopy, sounding, astronomy, surveillance, and also tactical systems, be it for ground application, airborne or spaceborne. The infrared Focal Plane Array (FPA), is a key part of the imaging system, and operated most of the time at cryogenic temperature (about 4 to 200 K), covering spectral bands in the range of 0.7 to 30 µm depending on technology. It is indeed composed of a pixelised sensing layer (this detection circuit being manufactured with dedicated material for the targeted IR wavelength, such as MCT, T2SL, QWIP InGaAs and InSb) which is hybridized via indium micro bumps onto a silicon Readout Integrated Circuit (ROIC), a mixed signal ASIC dedicated to the front end processing of the information generated by the pixels and to the multiplexing of related video signal information to be read out via few number of analogue, or more recently digital, output ports.

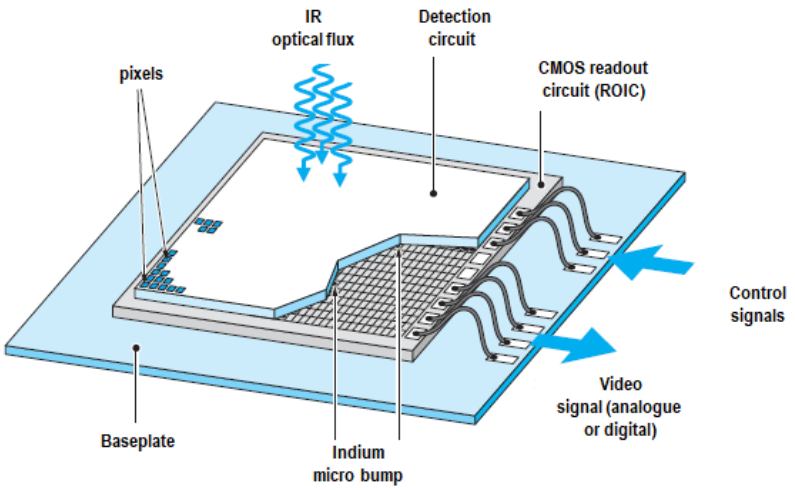
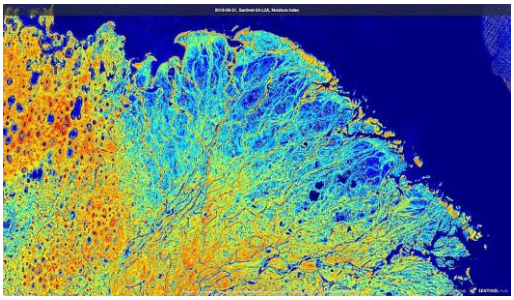


Figure 1 : Infrared Focal Plan Array schematic diagram [1]

This ROIC is designed and fabricated with a CMOS technology. Depending of the application, ROIC pixel pitches can range from hundreds of µm (e.g. for some space applications such as IASI-NG) to less than 10 µm (e.g. for tactical applications).

Sentinel-2 satellites carry a single multi-spectral instrument (MSI) with 13 spectral channels in the visible/near infrared (VNIR) and short wave infrared spectral range (SWIR)
https://commons.wikimedia.org/wiki/File:2019-08-31,_Sentinel-2A_L2A,_Moisture_index.jpg



Russia's Lena River Delta, a seen by the Sentinel 2 spacecraft on Aug. 31, 2019 in the near infrared and shortwave infrared. These wavelengths highlight the moisture content of vegetation

Example of surveillance picture from Teledyne FLIR detector

A Teledyne FLIR cooled detector for surveillance applications

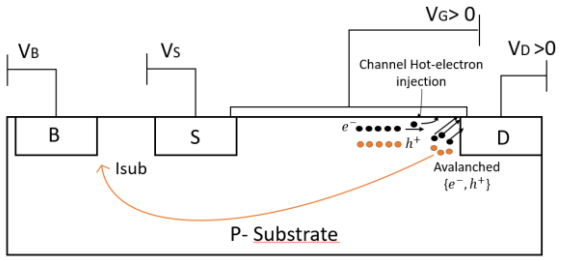
Figure 2 : Examples of applications and detector for IR imaging systems

As introduced above, the central role of the ROIC is to convert photocurrent, generated by pixels from the detection circuit when illuminated by an IR optical flux, into video signal and to format data to the outputs. The analog part of the ROIC is generally designed with mixed signal technology allowing the use of relatively high voltage (compared to fully digital technology) for the front end of readout chain in order to improve detector performances. This use of high voltage for the MOS transistors of the in-pixel readout chain implies high electric field generation in silicon and near gate oxide depending of the transistor biasing. This phenomenon leads to Hot Carrier Injection which degrades the device performances along time. The HCI degradation is well modeled at room temperature. However, at cryogenic temperature, this degradation is accentuated and no degradation model exists.

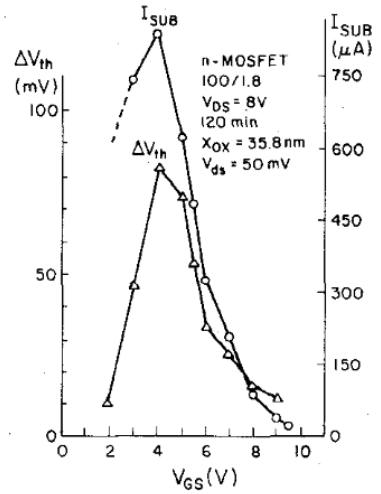
As mentioned below, the performances of InfraRed Focal Plane Array for space missions are impacted in several ways:

- Leakage current increase due to HCI impacts the performances of the transistors properties and can impact the End Of Life (EOL) detector performances for space applications. In extreme cases it can eventually lead to degradation of the device life time. As can be seen in Figure 3, the HCI degradation model and main mechanisms at ambient temperature are well known by silicon semiconductor foundries because it helps to determine the component lifetime and MTBF

(Mean Time Between Failure). However, no models exist at cryogenic temperatures where degradation needs to be assessed. Figure 1



Main mechanisms of hot-carriers injection in N-MOSFET under normal bias conditions ($V_G > 0$ and $V_D > 0$)

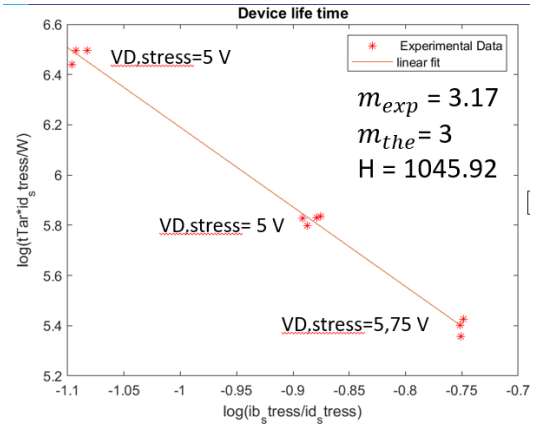


Relation between VTH degradation and bulk current increase of the MOSFET due to HCI REF [2] : Brian S. DOYLE and al

$$t_{Tar,use} = HW \frac{1}{I_{D,use}} \left(\frac{I_{B,use}}{I_{D,use}} \right)^{-m}$$

t_{TAR}: Time before failure
W: Parameter related to MOSFET
I_D, I_B: Drain and bulk current of the MOSFET
H, m: parameters extracted from MOSFET electrical measurements

Model equation allowing life time determination at ambient temperature REF [3] : Chenming HU and al

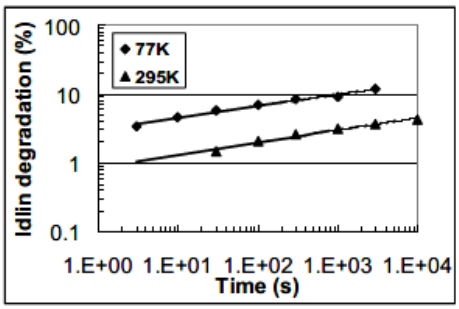


Example of measurements done at ISAE-SUPAERO for parameter extraction for life time determination at ambient temperature

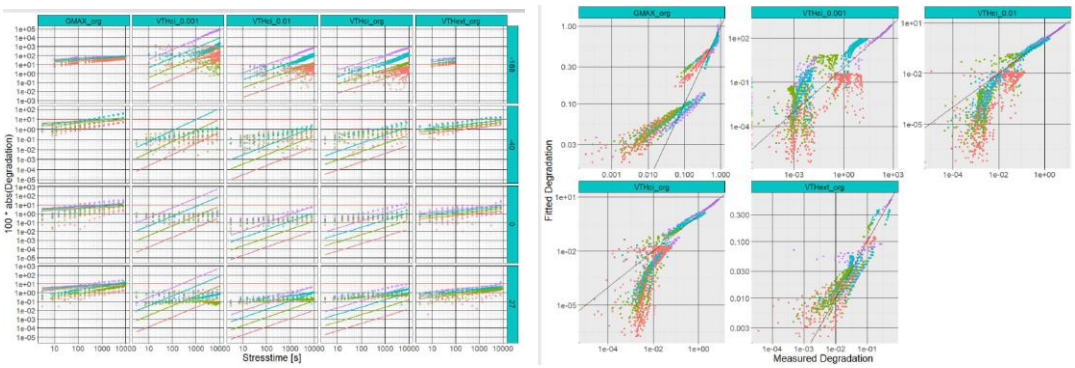
Figure 3 : Examples of HCI degradation and component lifetime determination

Figure 4 first an example of an available results on transistor parameter drift in literature balanced with other experimental results, slightly more complex, and the hot carrier injection drift associated fit vs experimental data which demonstrate existing law cannot allow to find a good acceleration set to all the transistor parameters. In addition, these single tests are limited at a minimum of 77K which is higher than the maximum operative temperature is some infrared detector. However, HCI considerations for cryogenic application requires a detailed knowledge of the product design, including the different building bricks sensitivity and operating condition, and some considerations about the acceleration factor. In addition, if one can determine how to assess HCI effect at technology single element, this can be more complex in ROIC circuit, as relevant for a space product, in the actual operating conditions which can be at lower

temperature than the one used to extract acceleration model. Indeed, while operating CMOS circuits at low temperature could improve performances (e.g. faster speed and lower stand-by power dissipation) and alleviate some failure mechanisms, HCI aging has been demonstrated as the primary CMOS reliability concern at cryogenic temperature. This is even more a concern for space than for most of other application domains (e.g. tactical one) because space IR detectors are most of the time nearly 100% on during several years. In addition, space is the main domain using VLWIR detectors (e.g. for meteorological, atmospheric physics and ground temperature measurement purposes) which are operated at a colder temperature with respect to MWIR or LWIR tactical detectors. Better mastering HCI effects on cooled space IR detectors would therefore be very valuable, on the one hand via the development of an accurate model for degradation prediction and on the other hand by validating mitigation techniques able to reduce HCI impacts on CMOS ROIC reliability.



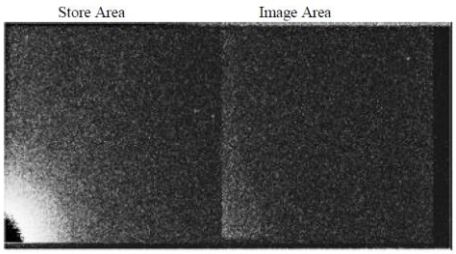
Example of degradation curve for a space FPA ROIC operated at 55K ; tests were limited at LN2 temperature of 77K (Franck Perrier, Anne Le paih, Lionel Dantas de Morais, Xavier Brenière "Cryogenic environment impacts on the reliability of infrared focal plan array" ISROS 2012 01-05 October 2012– Oral session)



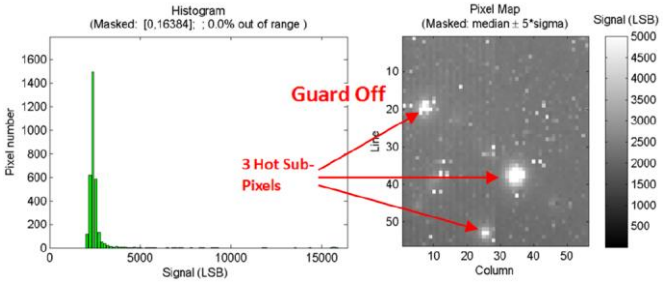
Example of HCI effect on transistor parameter drift used in detector ROIC assessment and associated fittings. Colors are reflecting the different drain voltage conditions as contributor to hot carrier injection drift. Curves on the right hand side picture are the showing the drift in each measured condition compared to the fit used

Figure 4 : Examples of degradation used for fitting parameter extraction

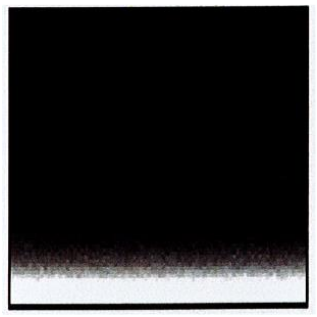
- The Figure 5 shows the glow and the blooming effects which are indirect consequences of the HCI generated by MOSFET contained in the readout circuit of a detector [4]-[7]. Indeed, HCI causes photon luminescence, also called electroluminescence which can add-up to the charges collected during integration time and bias measurements [8]. This is particularly true when detectors are used for low light flux and/or long integration time applications, such as in astronomy and low flux spectroscopy.



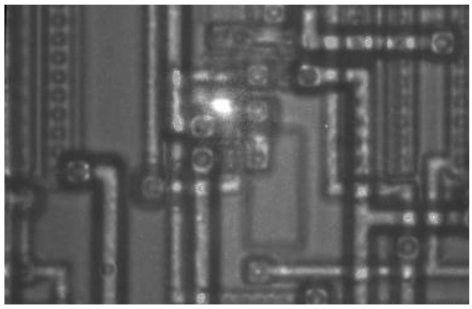
L3 CCD87 amplifier glow from [4]



Blooming example from [5] where carriers generated in three hot sub-pixels diffuse into neighboring pixels



High Gain Dark image with Ultrasat sensor (UV) showing the glow at the bottom rows for 5minutes integration time from [6]



Light emission from a transistor of a pixel in a static operation for CIS detector at ambient temperature (integration time: 60s) from [8]

Figure 5 : Examples of indirect impact of HCI with glow and blooming effects on detectors

- HCI phenomenon can also impact the Random Telegraph Noise (RTN) or Low Frequency Noise (LFN) behavior as depicted in Figure 7 and Figure 7 from [9]-[9]. Indeed, oxide traps created by HCI have a direct impact on LFN evolution of the MOSFET. In the past two years, a few works have been done to explore this impact mainly in CMOS image Sensors for visible wavelengths at room temperature (or around room temperature).

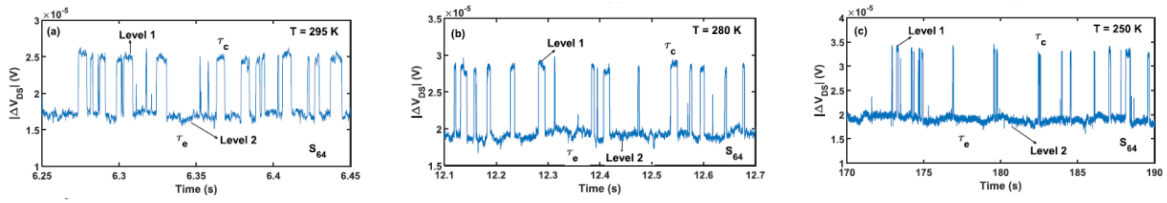


Figure 6 : Two-level RTS observed in MOSFET: Transition from level 1 to 2 represents the stress-induced trap S64 at VGS = -1.5 V after 500 s of stressing at (a) T = 295 K, (b) T = 280 K, and (c) T = 250 K (from [9])

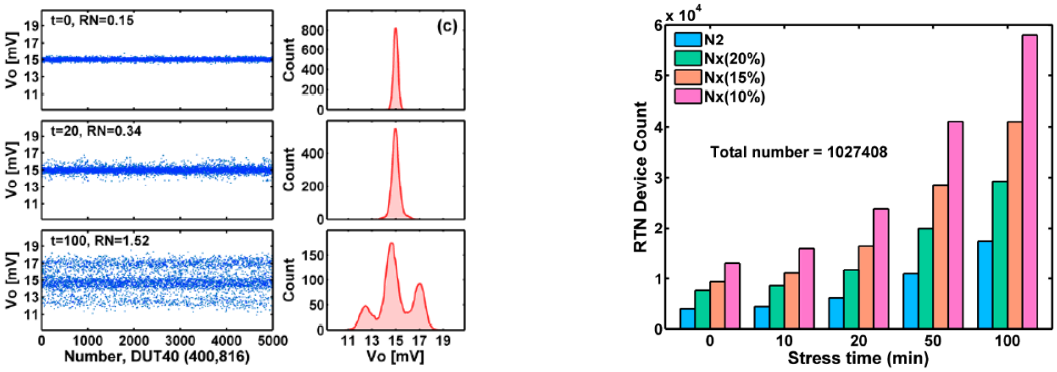


Figure 7 : Left: Generation of RTN traps during HCI stress. The 5000-frame waveforms before (t = 0) and after the HCI stress (t = 20, 100 min) with the corresponding histogram. Right: The count of RTN devices increases consistently as stress time increases. N2 is the number of devices showing two or more peaks in amplitude histograms. Nx is N2 plus the number of RTN like devices determined by setting the R-threshold to 10%, 15%, and 20%, respectively (from [10])

Objectives of the thesis:

The main objectives proposed for this PhD thesis work are as follows:

- After a bibliographic review covering the basic HCI mechanisms in silicon devices and the corresponding degradation (including degradation model) at ambient temperature, the doctoral student will explore the evolution of HCI impact on MOSFET devices for cryogenic temperature.
- This bibliographic work will be followed by an evaluation of the impact of these HCI phenomena on photonic detectors at room and cryogenic temperatures. This evaluation will be mainly focused on device life time, glow and blooming effects and RTN evolution.
- Identification of mitigation techniques which can reduce HCI impacts on detectors, especially for Infrared Focal Plane Arrays.
- Based on the requirements of space missions and mitigation techniques, the PhD student will define some devices which can be embedded in a test vehicle. A Design of Experiment (DoE) will be done to explore the limitations of these mitigation techniques and a performance estimation will be done by electrical simulations from the drawn layout done at low temperature (from 50K to 200K) and ambient temperature.
- Elaboration of a test setup which will be able to work a low temperature (from 50K to 200K) and ambient temperature, allowing to extract key performances of the device (and possible accelerating factors (as mentioned by Vincent they are weakly known?)
- From the measurement results done, the PhD student will conclude on the potential improvements to be implemented to enhance detector performances.
- The doctoral student will have to promote his/her results in the form of scientific publications and communications in international conferences.

Applicant Profile:

Master degree (or equivalent) in one or more of the following fields:

- Semiconductor device physics
- Solid state physics
- Nano/microelectronics (design, technology, manufacturing process…)
- Optoelectronics/Detectors
- Aerospace engineering

We are looking for self-motivated team-player candidates with excellent oral and written communication skills.

[1] Guérineau & al "Caractérisations électro-optiques des détecteurs plans focaux IR », Techniques de l'ingénieur (R6460)

[2] Brian S. DOYLE and al. "The Generation and Characterization of Electron and Hole Traps Created by Hole Injection During Low Gate Voltage Hot-Carrier Stressing of n-MOS Transistors," IEEE TRANSACTIONS ON ELECTRON DEVICES. VOL 37. NO. 8. AUGUST 1990

[3] Chenming HU and al. "Hot-Electron-Induced MOSFET Degradation— Model, Monitor, and Improvement," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-20, NO. 1, FEBRUARY1985

[4] Simon M. Tulloch, "Photon counting and fast photometry with L3 CCDs," Proc. SPIE 5492, Ground-based Instrumentation for Astronomy, (30 September 2004); https://doi-org.gorgone.univ-toulouse.fr/10.1117/12.550353

[5] S. Hanna, A. Bauer, H. Bitterlich, M. Bruder, L.-D. Haas, M. Haiml, K. Hofmann, K.-M. Mahlein, H.-P. Nothaft, T. Schallenberg, A. Weber, J. Wendler, R. Wollrab, J. Ziegler, "Two-dimensional focal plane detector arrays for LWIR/VLWIR space and airborne sounding missions," Proc. SPIE 7826, Sensors, Systems, and Next-Generation Satellites XIV, 78261H (13 October 2010); https://doi.org/10.1117/12.865836

[6] A. Birman and al, «5 Minutes IntegrationTime Deep UV Pixel Development for Ultrasat Space Mission», International Image Sensor Workshop 2023, IISW2015, 21-25 May 2023, Scotland

[7] F. Guellec, O. Boulade, C. Cervera, V. Moreau, O. Gravrand, J. Rothman, J-P Zanatta. "ROIC development at CEA for SWIR detectors: Pixel circuit architecture and trade-offs" ICSO 2014

[8] Stephan Maestre, Pierre Magnan, Francis Lavernhe, Franck Corbiere, "Hot carriers effects and electroluminescence in the CMOS photodiode active pixel sensors," Proc. SPIE 5017, Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications IV, (16 May 2003); https://doi.org/10.1117/12.476792

[9] T. Ahmed, Z. Çelik-Butler, F. -C. Hou, S. Tang and G. Mathur, "Identification of Channel Hot Carrier Stress-Induced Oxide Traps Leading to Random Telegraph Signals in pMOSFETs," in IEEE Transactions on Electron Devices, vol. 68, no. 2, pp. 713-719, Feb. 2021, doi: 10.1109/TED.2020.3044016.

[10] Chao, C.Y.-P.; Wu, T.M.-H.; Yeh, S.-F.; Lee, C.-L.; Tu, H.; Huang, J.C.-Y.; Chang, C.-H. Random Telegraph Noise Degradation Caused by Hot Carrier Injection in a 0.8 µm-Pitch 8.3Mpixel Stacked CMOS Image Sensor. Sensors 2023, 23, 7959. https://doi.org/10.3390/s23187959