PhD Position at
ISAE-SUPAERO & AIRBUS DS

Architecture analysis, exploration and design of in-pixel Digital ReadOut Integrated Circuit for InfraRed Focal Plane Array

PhD position proposed by ISAE-SUPAERO and Airbus Defense & Space

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Main location : ISAE-SUPAERO, Toulouse, France

Scientific field: Micro and Nanotechnology, Semiconductor Physics

Keywords: Digital readout circuit, circuit architecture, low temperature, microelectronic design

Context:

Nowadays, Infrared (IR) imaging systems are widely used in civilian and military settings through space and astronomy applications, surveillance, and also tactical systems. The infrared Focal Plane Array (FPA), is a key part of the imaging system, and operated most of the time at cryogenic temperature (50 to 200 K). It is composed of a pixelised sensing layer (this detection circuit being manufactured with dedicated material for the targeted IR wavelength, such as MCT, T2SL, QWIP and InSb) which is hybridized via indium micro bumps onto a Readout Integrated Circuit (ROIC), a mixed signal ASIC dedicated to the front end processing of the information generated by the pixels and to the multiplexing of related video signal information to be read out via few analogue or digital output ports.

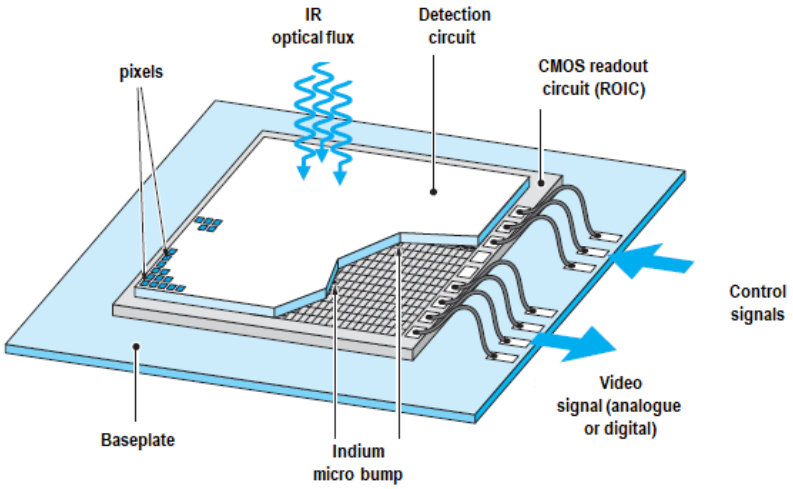
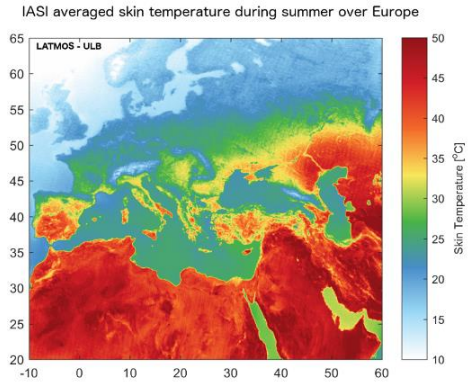


Figure 1 : Infrared Focal Plan Array schematic diagram [1]

This ROIC is designed and fabricated with a CMOS technology. Depending of the application, ROIC pixel pitches can range from hundreds of µm (e.g. for some space applications such as IASI-NG) to less than 10 µm (e.g. for tactical applications).

IASI-NG (Infrared Atmospheric Sounding Interferometer- Next Generation) instrument embedded in Metop-SG satellite



Example of map temperature from IASI instrument (Metop)

Example of surveillance picture from Teledyne FLIR detector

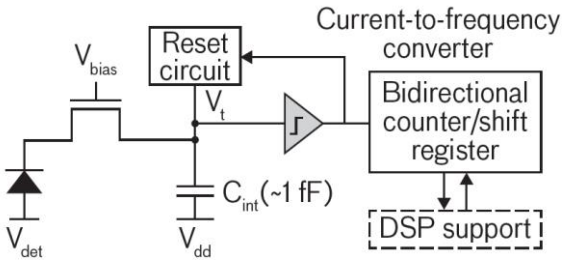
A Teledyne FLIR cooled detector for surveillance applications

Figure 2 : Examples of applications and detector for IR imaging systems

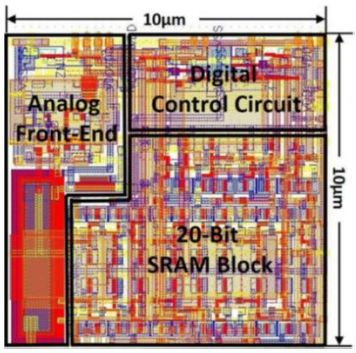
As introduced above, the central role of the ROIC is to convert photocurrent, generated by pixels from the detection circuit when illuminated by an IR optical flux, into video signal and to format data to the outputs. State of the art are now with digital outputs allowing an increase of data rate and a simplification of the associated external electronics. Most of these ROIC have an Analog to Digital Conversion (ADC) column architecture, like CMOS Image sensors for visible wavelengths applications in which a monolithic silicon bloc is used for detection and readout circuit.

In the past two decades, a few works [2]-[7] have been done to explore the possibility to integrate ADC into the ROIC pixel leading to several key advantages for most of infrared applications, including space ones:

- An increase of frame rate or a raise of pixel count (>20Mpixel)
- A decrease of power consumption due to decreasing voltage level when data is digitized
- An increase of the Signal to Noise Ratio (SNR) by increasing well charge and limiting quantization noise.
- A lower Low Frequency Noise impact (depending on architecture used)
- In-pixel pre-processing incorporation to extract relevant information

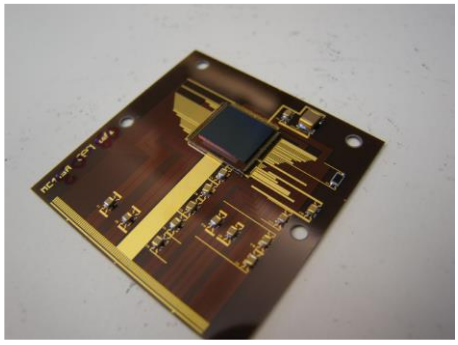


In-pixel ROIC ADC architecture,
REF [3] : Schultz & al (MIT US)



Layout of In-pixel ROIC ADC,
REF [5] : Javaid & al (Pak., S Arabia)

Layout of In-pixel ROIC ADC incorporating pre-processing, REF [2] : Shafique & al (Turkey)



FPA prototype mounted on PCB,
REF [6] : Bisotto & al (LETI France)

Figure 3 : Examples of works done on Digital ROIC

Objectives of the thesis:

The main objectives proposed for this PhD thesis work are as follows:

- After a bibliographic review covering the ADC architectures used in ROIC design (including CMOS image sensors), and ADC location, highlighting benefits and limitations, the PhD student will be able to identify the levers to exploit the different techniques in the different pixel pitch in the range of 10µm to 100 µm.
- Based on the requirements of space missions, the PhD student will define some in-pixel ROIC ADC architectures which can be embedded in a test vehicle. A Design of Experiment (DoE) will be done to explore the limitations of architectures designed and a performance estimation will be done by electrical simulations from the drawn layout done at low temperature (from 50K to 200K).
- Elaboration of a test setup which will be able to work a low temperature (from 50K to 200K) and allowing to extract key performances of the device
- From the measurement results done, the PhD student will identify the potential improvements to do for the in-pixel ADC to enhance performances
- The doctoral student will have to promote his/her results in the form of scientific publications and communications in international conferences.

Applicant Profile:

Master degree (or equivalent) in one or more of the following fields:

- Nano/microelectronics (design, technology, manufacturing process…)
- Optoelectronics/Detectors
- Semiconductor device physics
- Solid state physics
- Aerospace engineering

We are looking for self-motivated team-player candidates with excellent oral and written communication skills.

[1] Guérineau & al "Caractérisations électro-optiques des détecteurs plans focaux IR », Techniques de l'ingénieur (R6460)

[2] Guellec et al. "A 25 µm pitch LWIR focal plane array with pixel level 15 bits ADC providing high well capacity and targeting 2 mK NETD", Proc. SPIE 7660, 2010

[3] Shafique & al « Digital Pixel Readout Integrated Circuit Architectures for LWIR ». SPIE, 2015. https://doi.org/10.1117/12.2177551

[4] Schultz & al « Digital-Pixel Focal Plane Array Technology », LINCOLN LABORATORY JOURNAL VOLUME 20, NUMBER 2, 2014

[5] Ito & al « A Computational Digital Pixel Sensor Featuring Block-Readout Architecture for On-Chip Image Processing ». *IEEE Transactions on Circuits and Systems I: Regular Papers* 56, n° 1 (janvier 2009): 114-23. https://doi.org/10.1109/TCSI.2008.926983

[6] Javaid & al. « A Configurable High Resolution Digital Pixel Readout Integrated Circuit with On-Chip Image Processing ». *Computers & Electrical Engineering* 86 (septembre 2020): 106720. https://doi.org/10.1016/j.compeleceng.2020.106720

[7] Bisotto & al « A 25µm Pitch LWIR Staring Focal Plane Array with Pixel-Level 15-Bit ADC ROIC Achieving 2mK NETD ». SPIE 2010. https://doi.org/10.1117/12.865062