**INTERNSHIP DESCRIPTION**

**Domain:**
DIGITAL ELECTRONIC

**Title:**
DESIGN AND IMPLEMENTATION OF AN ETHERNET SWITCH IN A FPGA

**Context:**
The department of complex system engineering of ISAE-SUPAERO is developing a new network aimed at ensuring reliability, low jitter and latencies, without the need for synchronization or complex network planning[1]. This network, called Factoring, is Time Sensitive Network compliant[2] at 1Gbit/s, based on an interface called T-Factoring or T for short, that allows any Ethernet-compliant equipment to exchange data via the network. Several articles and patents have already been filed for this project.

**Objectives:**
The purpose of this internship is to design and implement a bridge, called a gateway, between 2 Factoring networks. This bridge will extend the Factoring base network to a more complex topology. A large part of the gateway functions already exist in the T. The first part of the internship will therefore consist of analyzing the existing code, and extracting the reusable functions.

**Tasks:**
To successfully complete this project, the intern will have to, with the support of the project team, carry out the following tasks:
- Analysis of existing code
- Definition of an FPGA architecture to carry out the main functions:
  - Building the routing table
  - Sorting and forwarding Ethernet frames to the right destination
  - Reconfiguring the gateway when a failure is detected
- VHDL reuse and design (synthesizable code)
- Creation/modification of Test-Bench(s) for virtual verification
- Placement and routing on Xilinx FPGA target
- Validation of the FPGA on a model representative of the final product
- Writing a technical report.

**References:**

Application: please send us by email a curriculum vitae.
Application deadline: February 15th, 2024
Location: ISAE, Campus SUPAERO (Toulouse, France)
Duration: 5 months, starting March or April, 2024

**APPLICANT PROFILE**
Knowledge and required level: M2 level, knowledge on digital electronic, VHDL, computer programming