





POST-DOCTORAL POSITION Digital design and signal processing for satellite optical communication systems

CONTEXT:

Digital optical telecommunications have made it possible to build very high-speed terrestrial fiber networks, but microwaves are still the main physical layer in satellite communications. While optics have proved their worth on inter-satellite links, satellite-to-ground optical transmissions are currently being considered as part of the equipment for new platforms, particularly those for new satellite constellation programs. The advantages are identical to those of terrestrial links: very high data rate, directional beam, secure communications. Future generations of high-capacity satellites (SATCOM) in low earth orbit (LEO) and geostationary orbit (GEO) will have to include an optical component to guarantee increased throughput. However, the robustness and resilience of the link are highly dependent on atmospheric conditions, in particular cloud cover, optical background noise and atmospheric turbulence. In LEO, the Doppler effect will also have an impact on data availability. All these disturbances compromise the reliability of the link and degrade the signal-to-noise ratio. Various transmitted waveforms and different types of detection have been studied, but complex modulation formats (QPSK, 8PSK, etc.) and coherent detection, as for terrestrial networks, are proving to be the most effective, at the expense of more complicated implementation (sensitivity to frequency fluctuations). The CALICO project proposes to study and design a new coherent detection technique at the interface between optics and digital electronics in order to compensate for the Doppler effect and improve the detection threshold. The objectives are to design a phaselocked loop to recover the phase and amplitude of the signal. To achieve this, an original hybrid approach will be used to recover a carrier and a signal that are as clean as possible as soon as they leave the physical and electronic layer. It involves combining an optical phase-locked loop (OPLL) with digital processing on a DSP.

MISSION :

The post-doctoral researcher will contribute to the CALICO project, focusing on the development and optimization of advanced detection techniques for optical satellite communications. Their responsibilities will include:

- 1. Design and Implementation of Control Loop Hardware Architecture
 - Develop the hardware architecture for a control loop, from a Simulink model, that integrates an optical phase-locked loop (OPLL) with digital signal processing (DSP).
 - Translate simulation models into optimized hardware designs using VHDL for FPGA implementation.
- 2. Simulation and Optimization of Hardware Models
 - Simulate the control loop using advanced modeling tools to evaluate performance under varying conditions, including Doppler shifts, atmospheric turbulence, and noise.
 - Optimize the design to ensure robust operation and low error rates in challenging environmental conditions.

- 3. Real-Time System Testing on Laser Test Bench
 - Conduct real-time tests of the hardware on a dedicated laser test bench to validate system functionality and performance.
 - Develop testing protocols and adapt the system to ensure compatibility with experimental setups.
- 4. Analysis and Scientific Contribution
 - Analyze test results to assess the performance of the control loop and identify areas for further improvement.
 - Collaborate with the research team to synthesize findings into scientific publications and present results at relevant conferences.

This role offers a unique opportunity to contribute to cutting-edge research at the interface of optics and digital electronics, with potential applications in next-generation satellite communication systems.

DURATION :

18 months

CANDIDATE'S PROFILE :

Note that the selected candidate has to be validated by the DGA (French Government Defence procurement and technology agency), an European nationality is mandatory.

We are seeking a highly motivated post-doctoral researcher with a strong background in digital design and signal processing for telecommunications, specifically in high-speed satellite optical communication systems. The ideal candidate will possess the following qualifications and skills:

- A Ph.D. in Electrical Engineering, Telecommunications, Signal Processing, or a related field.
- Expertise in digital hardware design, including hands-on experience in VHDL/Verilog and FPGA programming.
- Strong understanding of signal processing techniques for telecommunications, with a focus on modulation formats (e.g., QPSK, 8PSK) and coherent detection methods.
- Experience in designing and implementing control loops, including phase-locked loops (PLLs).
- Proficiency in simulation and modeling tools such as MATLAB, Simulink, or equivalent.
- Familiarity with real-time system testing and debugging in laboratory environments.
- Ability to analyze and interpret experimental results to identify areas for optimization.
- Strong written and verbal communication skills, with the ability to contribute to scientific publications.

The candidate should demonstrate a proactive and innovative mindset, capable of working independently while collaborating effectively within a multidisciplinary team.

Please send a cover letter, a CV detailing the experience to: Arnaud DION <u>arnaud.dion@isae-supaero.fr</u> Fabien DESTIC <u>fabien.destic@isae-supaero.fr</u>