DIGITAL ELECTRONIC ENGINEER

CONTEXT :

Digital optical telecommunications have made it possible to build very high-speed terrestrial fiber networks, but microwaves are still the main physical layer in satellite communications. While optics have proved their worth on inter-satellite links, satellite-to-ground optical transmissions are currently being considered as part of the equipment for new platforms, particularly those for new satellite constellation programs. The advantages are identical to those of terrestrial links: very high data rate, directional beam, secure communications. Future generations of high-capacity satellites (SATCOM) in low earth orbit (LEO) and geostationary orbit (GEO) will have to include an optical component to guarantee increased throughput. However, the robustness and resilience of the link are highly dependent on atmospheric conditions, in particular cloud cover, optical background noise and atmospheric turbulence. In LEO, the Doppler effect will also have an impact on data availability. All these disturbances compromise the reliability of the link and degrade the signal-to-noise ratio. Various transmitted waveforms and different types of detection have been studied, but complex modulation formats (QPSK, 8PSK, etc.) and coherent detection, as for terrestrial networks, are proving to be the most effective, at the expense of more complicated implementation (sensitivity to frequency fluctuations). The CALICO project proposes to study and design a new coherent detection technique at the interface between optics and digital electronics in order to compensate for the Doppler effect and improve the detection threshold. The objectives are to design a phase-locked loop to recover the phase and amplitude of the signal. To achieve this, an original hybrid approach will be used to recover a carrier and a signal that are as clean as possible as soon as they leave the physical and electronic layer. It involves combining an optical phase-locked loop (OPLL) with digital processing on a DSP.

MISSION :

The selected candidate will play a key role in the CALICO project, contributing to the development of advanced detection systems for optical satellite communications. Their responsibilities will include:

1. **Digital Hardware Development for Control Loop Architecture**
   - Support the development of a hardware architecture for a control loop, translating simulation models into VHDL-based designs for FPGA implementation.
   - Collaborate with the team to integrate optical and digital signal processing components into a coherent system.
2. **Simulation and Testing of Hardware Designs**
   - Use simulation tools such as MATLAB or Simulink to evaluate the performance of control loop models under realistic environmental conditions (e.g., Doppler effects, noise, atmospheric turbulence).
   - Optimize the design for robustness and accuracy in challenging satellite communication scenarios.
3. **Hands-On Real-Time System Testing**
   - Conduct real-time tests of the hardware on a laser test bench, working closely with the research team to validate system performance.
   - Assist in troubleshooting and fine-tuning the hardware to ensure reliable operation.

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4. **Data Analysis and Reporting**
    - Analyze test data to evaluate the effectiveness of the system and identify opportunities for improvement.
    - Prepare technical documentation and reports detailing the findings and results of experiments.
5. **Collaboration and Innovation**
    - Work within a multidisciplinary team of engineers and researchers, contributing ideas and solutions to overcome technical challenges.
    - Stay informed about the latest advances in satellite communications and digital electronics, applying innovative approaches to the project.

This position offers a unique opportunity to contribute to state-of-the-art research and development in satellite optical communication systems, with potential for significant technical and professional growth.

DURATION :

18 months

CANDIDATE'S PROFILE :

Note that the selected candidate has to be validated by the DGA (French Government Defence procurement and technology agency), an European nationality is mandatory.

We are seeking a motivated master's graduate or junior engineer with a strong interest in digital hardware design and signal processing for telecommunications. The ideal candidate will possess the following qualifications and skills:

- A master's degree or equivalent in Electrical Engineering, Digital Electronics, Telecommunications, or a related field.
- Practical experience in digital hardware design, including proficiency in VHDL for FPGA programming, gained through academic projects, internships, or professional experience.
- Understanding of signal processing concepts, particularly in modulation techniques (e.g., QPSK, 8PSK) and coherent detection methods.
- Experience in simulation and modeling tools such as MATLAB, Simulink, or equivalent.
- Familiarity with basic control loop principles, such as phase-locked loops (PLLs), is desirable but not mandatory.
- Ability to work effectively within a team while showing initiative and resourcefulness in problem-solving.
- Eagerness to learn and contribute to cutting-edge satellite communication projects.

This position is an excellent opportunity for a recent graduate or early-career professional to gain hands-on experience in the field of digital telecommunications and satellite systems.

Please send a cover letter, a CV detailing the experience to:

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