

Toulouse



INTERNSHIP OFFER 3 – 4 months (Summer 2023)

 \mathbb{Z}

jerome.puech@isae.fr; marc.justicia-mayoral@isae.fr

Design HIL link between simulation software and On-Board-Computer

Description

Hardware-In-the-Loop testing is a crucial step when it comes to satellite design V&V. Flight software shall be tested directly on the real on-board computer, while the space environment is emulated. HIL testing saves time and money in many situations. In space applications, they make it possible to test the FSW without implementing large test resources.

The space environment will be simulated with an open-source solution called Basilisk (<u>http://hanspeterschaub.info/basilisk/</u>) and the flight software is based on LVCUGEN from CNES.

Internship results expected

The goal of the internship will be to design the interface between the simulator and the on-board computer. Some design steps are expected:

1° Develop the needed classes in the simulator (e.g. a temperature sensor, a reaction wheel, ...)

2° Check the feasibility with an ethernet link (data rate limitations, TCP/UDP feasibility, ...)

3° Program the link between the simulator and OBC (one data stream bus of I2C or 1Wire from OBC to PC).

Skills and prerequisites

Preparation of a diploma in Engineering (software development / electronics), Bac +4/+5.

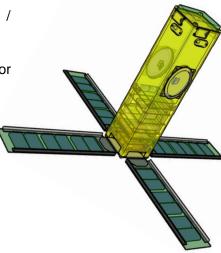
- Strong knowledge of programming languages (Python and/or C/C++)
- Basic knowledge of network communication protocols
- Model Based Design
- A good knowledge in space application would be a plus
- Autonomy and proactivity

Language skills

- English mandatory
- French and/or Spanish accepted

How to apply?

Send resume to jerome.puech@isae.fr and marc.justicia-mayoral@isae.fr.



ISAE SUPAERO - Institut Supérieur de l'Aéronautique et de l'Espace

10, avenue Edouard-Belin - BP 54032 - 31055 Toulouse CEDEX 4 - FRANCE Tél : 33 (0)5 61 33 80 80 - Télécopie : 33 (0)5 61 33 83 30 - Site internet : www.isae-supaero.fr